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(71) Applicants: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). **ANALOG DEVICES, INC.** [US/US]; One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (US).

(72) Inventors: **ROTH, Charles, P.**; 13305 Tichester Court, Austin, TX 78729 (US). **SINGH, Ravi, P.**; 12349 Metric Boulevard, #829, Austin, TX 78758 (US). **KOLAGOTLA, Ravi**; 11500 Jollyville Road, #1823, Austin, TX 78759 (US). **DINH, Tien**; 1918 Coachlamp Drive, Cedar Park, TX 78613 (US).

(74) Agent: **HARRIS, Scott, C.**; Fish & Richardson P.C., 4350 La Jolla Village Drive, Suite 500, San Diego, CA 92122 (US).

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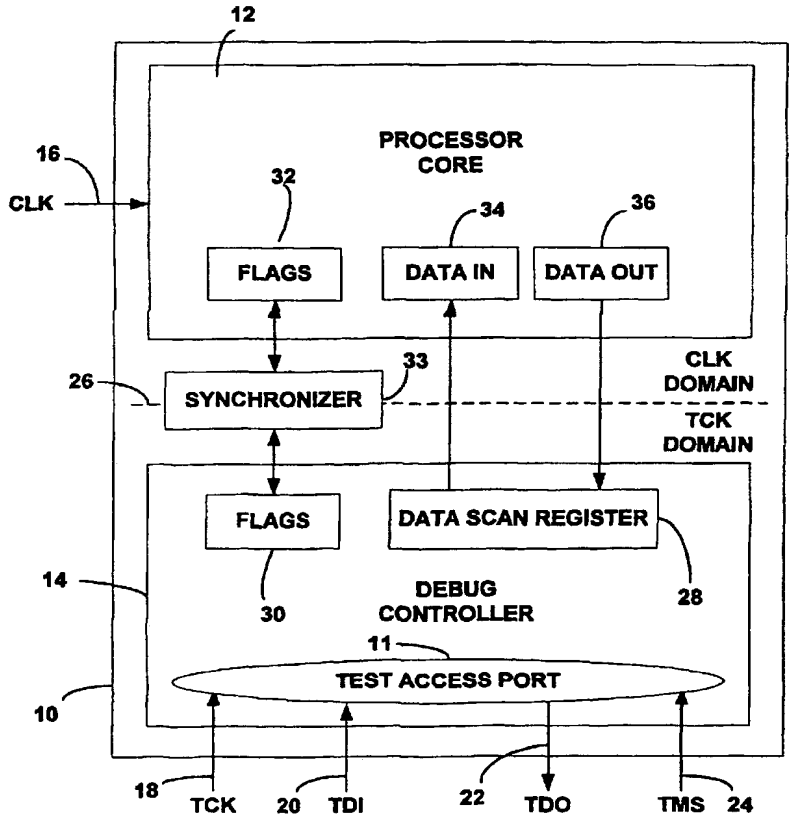
(54) Title: DATA SYNCHRONIZATION FOR A TEST ACCESS PORT



(57) Abstract: In one embodiment, an integrated circuit provides a test access port that communicates with scan chain registers in a processor core. The integrated circuit synchronizes data transferred between a debug controller that operates under control of a test clock (TCK) and the processor core that operates under control of a processor clock (CLK).

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